CLAIMS

1. A method of manufacturing an electronic device including a thin film transistor, comprising the steps of:

(a) forming a semiconductor film over an insulating substrate;

(b) depositing a first masking layer over the semiconductor film and removing portions thereof to form a plurality of holes therethrough which extend substantially perpendicularly from the upper to the lower surface thereof;

(c) patterning the first masking layer in a first pattern;

(d) depositing a second masking layer over the first masking layer;

(e) patterning the second masking layer to define a second pattern that lies within the area of the first pattern; and

(f) implanting the semiconductor film using at least the first masking layer as an implantation mask, with a portion of the first masking layer which defines at least some of the holes partially masking the implantation, such that the implantation defines source and drain regions an undoped conduction channel between the source and drain regions, and a field-relief region having a lower doping concentration than the drain region between the conduction channel and the drain region.

2. A method of Claim 1 wherein step (b) comprises providing an array of spaced raised features over the semiconductor film depositing the first masking layer thereover, and removing the raised features together with the portions of the first masking layer material overlying the raised features.

3. A method of Claim 1 wherein step (b) comprises depositing a first masking layer over the semiconductor film defining an etchant mask over the first masking layer, and etching a plurality of holes through the material of the first masking layer.

4. A method of Claim 3 wherein step (c) is carried out before the step of etching holes in the first masking layer.

5. A method of Claim 3 wherein the step of etching holes in the first masking layer is carried out after step (e), such that the holes are formed through the exposed areas of the first masking layer.

6. A method of Claim 1 wherein step (d) is carried out before step (c), and the method includes a further step (h) after step (d) and before step (c) of patterning the second masking layer to form a mask in the first pattern for the patterning of the first masking layer in step (c).

7. A method of Claim 6 wherein step (h) comprises defining the second pattern in the second masking layer and then forming sidewall spacers adjacent the second masking layer to define the first pattern.

8. A method of Claim 1 wherein step (e) comprises defining the second pattern in a third masking layer over the second masking layer oxidising the exposed portions of the second masking layer, and then removing the oxidised portions of the second masking layer thereby defining the second pattern in the second masking layer.

9. A method of Claim 1 wherein the first masking layer forms a gate insulating layer and the second masking layer forms a gate electrode layer.

10. A method of Claim 1 wherein the first masking layer forms a gate electrode layer, and the method includes a step of depositing a gate insulator layer after step (a) and before step (b).

11. An electronic device including a thin film transistor fabricated according to a method of Claim 1.

12. An electronic device including a thin film transistor which comprises a patterned semiconductor film on an insulating substrate a gate insulator layer over the semiconductor film, and a gate electrode over the gate insulator layer, the semiconductor film comprising source and drain regions an undoped conduction channel between the source and drain regions, and a field-relief region having a lower doping concentration than the drain region between the conduction channel and the drain region, wherein a portion of the gate electrode overlaps the field-relief region and has a plurality of holes defined therethrough which extend substantially perpendicularly from the upper to the lower surface thereof.

13. A device of Claim 12 wherein the length of the field-relief region is less than 1μm.

14. A device of Claim 12 wherein the holes in the first masking layer expose around 1 to 10% of the underlying layer.

15. A device of Claim 12 wherein the average hole diameter is less than 100nm.

16. An electronic device including a thin film transistor which comprises a patterned semiconductor film on an insulating substrate a gate insulator layer over the semiconductor film and a gate electrode over the gate insulator layer, the semiconductor film comprising source and drain regions an undoped conduction channel between the source and drain regions, and a field-relief region having a lower doping concentration than the drain region between the conduction channel and the drain region, wherein a portion of the gate insulator layer overlaps the field-relief region and has a plurality of holes defined therethrough which extend substantially perpendicularly from the upper to the lower surface thereof, and the gate electrode is self-aligned with the conduction channel.

17. A device of Claim 16 wherein the length of the field-relief region is less than 1μm.

18. A device of Claim 16 wherein the holes in the first masking layer expose around 1 to 10% of the underlying layer.

19. A device of Claim 16 wherein the average hole diameter is less than 100nm.